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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,549	02/27/2004	Chang-Ho Do	51876P595	7064

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EXAMINER	
CUNNINGHAM, TERRY D	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,549	DO, CHANG-HO	
	Examiner	Art Unit	
	Terry D. Cunningham	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-17* is/are rejected.

7)☒ Claim(s) *18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of changes in this action

1. The indefiniteness rejection to claims 2, 4 and 12 has been overcome responsive to the amendment.
2. The rejection to claims 1, 2 and 11 under 35 U.S.C. § 102 has been overcome responsive to the amendment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1, 2 and 5-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh (USPN 4,902,910) in view of Lovett (USPN 5,889,416). The reference to Hsieh discloses, in Fig. 8, a circuit similar to that recited in the claims. However, the Hsieh does not teach the express details for the NAND gate 83 of Fig. 8. The reference to Lovett discloses, in Fig. 13, an improved NAND gate having the benefit of uniform slew rate. Therefore, it would have been obvious for one skilled in the art to use the specific NAND gate taught in Fig. 13 of Lovett for the broad NAND gate 83 of Fig. 8 of Hsieh to obtain the expected advantage of uniform slew rate in the NAND gate.

This combination to Hsieh and Lovett would provide a circuit comprising: "a power supply voltage level follower unit (4-1A of Hsieh)"; "a power supply voltage detection unit (4-

2A of Hsieh)"; "a detection signal (4C' of Hsieh)"; "a reset prevention unit (80 and 83, wherein the circuit of Fig. 13 of Lovett is used for 83)" having "a power-up signal (POR)", "a first pull-up means (1008 of Fig. 13 of Lovett)", "a first pull-down means (1016 of Fig. 13 of Lovett)", "delay unit (80 of Hsieh)" and "a second pull-up means (1002 of Fig. 13 of Lovett)". Reference is made to Fig. 9 of Hsieh that shows the corresponding operation. As seen, the "power-up signal" during times t4 through t6+td is a "pull-down signal" that is generated (i.e., pulled-down) by NAND gate 83". NAND gate 83 is "controlled by the detection signal (4C') and a delayed detection signal (4D')" as well as signal 4F'. Further, the signal POR is prevented "from transitioning during a power drop of the power supply voltage" when the drop has a duration less that a predetermined value. Thus, the combination provides the recited operation.

With respect to claim 12, the "pull-down means" and the "first pull-up means" would be 1016 and 1008, respectively. The "second pull-up means" would be 1002.

With respect to claims 13-15, it is notoriously well known to control phase and logic level of an output signal using one or more inverter buffers depending on the amount of phase or logic level desired. Therefore, it would have been obvious for one skilled in the art to add inverter buffer for our signal POR to obtain the expected advantage of adjusting the phase of logic level.

Examiner has fully considered Applicant's remarks for the above rejection and has not found them to be persuasive. Initially, Applicant appears to be relying on the remarks for the rejection to claims 1, 2 and 11 to under 35 U.S.C. § 102, if view of Hsieh alone to traverse the rejection under 35 U.S.C. § 103 in view of the combination of Hsieh in view of Lovett. However, the claims were rejected under 35 U.S.C. § 102 for different reasons than under 35 U.S.C. § 103. Thus, the remarks cannot be found to be persuasive.

Applicant further remarks "...the Examiner is correct that a NAND gate can incorporate pull-up and pull-down transistors. However, the reset prevention unit including pull-up means and pull-down means connected and controlled as recited in claim 1 does not implement a NAND function". It is not understood how this is relevant. Even with the "NAND gate", the above makes its clear that the combination includes the recited elements having the recite connections and operation.

Claims 18 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 571-272-1742. The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
Primary Examiner
Art Unit 2816

TC
March 28, 2006